CLAIMS

[0076] What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A photodiode for use in an imaging device, said photodiode comprising:

a first layer of a first conductivity type formed in a substrate and laterally displaced from an electrically active portion of gate of a charge transfer transistor by a distance of about 0 Angstroms to about 5,000 Angstroms; and

a charge collection region of a second conductivity type formed below said first layer for accumulating photo-generated charge, said charge collection region being adjacent said transistor gate, said gate transferring charge accumulated in said charge collection region to a doped region of said second conductivity type.

2. The photodiode of claim 1, wherein said first layer is laterally displaced from said electrically active portion by about 300 Angstroms to about 3,000 Angstroms.

3. The photodiode of claim 1, wherein said first layer is a surface layer.

4. The photodiode of claim 1, wherein said first layer is in contact with an isolation region formed within said substrate.

5. The photodiode of claim 1, wherein said first conductivity type is p-type and said second conductivity type is n-type.

6. The photodiode of claim 5, wherein said first layer is doped with a p-type dopant at an implant dose of from about 1 x 10^{12} to about 1 x 10^{14} atoms per cm^2.

7. The photodiode of claim 5, wherein said charge collection region is doped with an n-type dopant at an implant dose of about 1 x 10^{11} to about 1 x 10^{14} atoms per cm^2.

8. The photodiode of claim 1, wherein said photodiode is a p-n-p photodiode.

9. The photodiode of claim 1, wherein said imaging device is one of a 3T, 4T, 5T or 6T imaging device.

10. The photodiode of claim 1, wherein said imaging device is a CCD imaging device.

11. An image pixel comprising:

a gate structure of a transistor formed over a semiconductor substrate; and

a photodiode adjacent said gate, said photodiode comprising a pinned layer of a first conductivity type and a doped region of a second conductivity type located below said pinned layer, said pinned layer being laterally displaced from an electrically active portion of said gate by a distance of about 0 Angstroms to about 5,000 Angstroms, and said doped

region being spaced from said electrically active portion of said gate by a gate sidewall.

12. The image pixel of claim 11, wherein said pinned layer is laterally displaced from said gate by a distance of about 300 Angstroms to about 3,000 Angstroms.

13. The image pixel of claim 11, wherein said pinned layer is adjacent and in contact with an isolation region formed within said semiconductor substrate.

14. The image pixel of claim 11, wherein said first conductivity type is p-type and said second conductivity type is n-type.

15. The image pixel of claim 11, wherein said pinned layer is doped with dopants selected from the group consisting of boron, beryllium, indium and magnesium.

16. The image pixel of claim 11, wherein said pinned layer is doped with boron at an implant dose of from about 1 x 10^{12} to about 1 x 10^{14} atoms per cm^2.

17. The image pixel of claim 11, wherein said photodiode is a p-n-p photodiode.

18. The image pixel of claim 11, wherein said photodiode is part of a CMOS imager.

19. The image pixel of claim 11, wherein said photodiode is part of a CCD imager.

20. A photodiode of an image sensor comprising:

a surface layer of a first conductivity type adjacent a gate of a transfer transistor, said gate being formed over a silicon substrate; and

a doped region of a second conductivity type located below said surface layer, at least a portion of said doped region being located between said gate and said surface layer, said pinned layer being laterally displaced from said gate by a distance of about 0 Angstroms to about 5,000 Angstroms.

21. The photodiode of claim 20, wherein said surface layer is laterally displaced from said gate by a distance of about 300 Angstroms to about 3,000 Angstroms.

22. The photodiode of claim 20, wherein said surface layer is adjacent and in contact with an isolation region formed within said silicon substrate.

23. The photodiode of claim 20, wherein said surface layer and said doped region are both located within a doped layer of said first conductivity type.

24. The photodiode of claim 20, wherein said surface layer is doped with phosphorous at an implant dose of from about 1×10^{12} to about 1×10^{14} atoms per cm^2.

25. The photodiode of claim 20, wherein said image sensor is a CMOS imager.

26. The photodiode of claim 20, wherein said image sensor is a CCD imager.

27. A CMOS imager system comprising:

(i) a processor; and

(ii) a CMOS imaging device coupled to said processor, said CMOS imaging device comprising:

a field isolation region formed in a substrate; and

a pixel adjacent said field isolation region, said pixel comprising a p-n-p photodiode adjacent a gate of a transfer transistor, said p-n-p photodiode further comprising a p-type surface layer and an n-type doped region located below said p-type surface layer, said p-type surface layer being laterally displaced from an electrically active portion of said gate by a distance of about 0 Angstroms to about 5,000 Angstroms.

28. The system of claim 27, wherein said p-type surface layer is laterally displaced from said electrically active portion of said gate by about 300 Angstroms to about 3,000 Angstroms.

29. The system of claim 27, wherein said p-type surface layer is adjacent and in contact with said field oxide region.

30. The system of claim 27, wherein said p-type surface layer and said n-type doped region are both located within a p-type doped region.

31. The system of claim 27, wherein said p-type surface layer is doped with boron at an implant dose of from about 1 x 10^{12} to about 1 x 10^{14} atoms per cm^2.

32. A method of forming a photodiode for a pixel sensor cell, said method comprising:

forming a gate of a transistor over a substrate;

forming a first doped layer of a first conductivity type in said substrate, said first doped layer being displaced laterally from an electrically active portion of said gate by a predetermined distance; and

forming a doped region of a second conductivity type in said substrate and below said first doped layer by implanting ions of said second conductivity type in a first direction and at an incidence angle with said substrate different than a zero degree angle in a first area of said substrate below said first doped layer.

33. The method of claim 32, wherein said first doped layer is formed by implanting ions of said first conductivity type at an incidence angle with said substrate different than a zero degree angle.

34. The method of claim 32, wherein said first doped layer is formed by implanting ions of said first conductivity type at an incidence angle with said substrate of about zero degree angle.

35. The method of claim 32, wherein said first direction is a right-to-left direction relative to said gate and into said substrate.

36. The method of claim 32, wherein said first doped layer has an implant dose within the range of from about 1×10^{12} to about 1×10^{14} atoms per cm^2.

37. The method of claim 32, wherein said first doped layer is formed to be laterally displaced from said electrically active portion of said gate by about 0 Angstroms to about 5,000 Angstroms.

38. The method of claim 37, wherein said first doped layer is formed to be laterally displaced from said electrically active portion of said gate by about 300 Angstroms to about 3,000 Angstroms.

39. The method of claim 32, wherein said act of forming said first doped layer further comprises forming a photoresist layer over said substrate and said gate, and patterning and etching said photoresist layer to expose a second area of said substrate, said second area being located between said gate and said at least one isolation region, said second area being spaced from said gate by said predetermined distance.

40. The method of claim 32, wherein said act of forming said doped region of said second conductivity type further

comprises forming a photoresist layer over said substrate and said gate, and patterning and etching said photoresist layer to expose said first area of said substrate located between a sidewall of said gate and said at least one isolation region.

41. The method of claim 32, wherein said act of implanting ions of said second conductivity type further comprises directing a dopant at said incidence angle which is different than a zero degree angle in said first area of said substrate located between said gate and said at least one isolation region.

42. The method of claim 32, wherein said doped region has an implant dose within the range of from about 1×10^{11} to about 1×10^{14} atoms per cm^2.

43. The method of claim 32, wherein said first conductivity type is p-type and said second conductivity type is n-type.

44. The method of claim 32, wherein said photodiode is a p-n-p photodiode.

45. The method of claim 32, wherein said photodiode is part of a CMOS imager.

46. The method of claim 32, wherein said photodiode is part of a CCD imager.

47. A method of forming a photodiode, said method comprising:

forming at least one shallow trench isolation region in a silicon substrate;

forming a transistor gate over said silicon substrate and spaced apart from said at least one shallow trench isolation region;

forming a first doped layer of a first conductivity type in said silicon substrate;

forming a second doped layer of said first conductivity type in said first doped layer by implanting ions in a first direction and at an incidence angle with said silicon substrate other than zero degrees, said second doped layer being in contact with said isolation region and being displaced laterally from an electrically active area of said transistor gate by a predetermined distance; and

forming a doped region of a second conductivity type in said first doped layer by implanting ions in a second direction and at an incidence angle with said silicon substrate other than zero degrees.

48. The method of claim 47, wherein said second doped layer has an implant dose within the range of from about 1×10^{12} to about 1×10^{14} atoms per cm^2.

49. The method of claim 47, wherein said second doped layer is laterally displaced from said electrically active area of said

transistor gate by about 0 Angstroms to about 5,000 Angstroms.

50. The method of claim 49, wherein said second doped layer is laterally displaced from said electrically active area of said transistor gate by about 300 Angstroms to about 3,000 Angstroms.

51. The method of claim 47, wherein said act of forming said doped region further comprises forming at least a portion of said doped region between said second doped layer and said transfer gate.

52. The method of claim 47, wherein said doped region has an implant dose within the range of from about 1×10^{11} to about 1×10^{14} atoms per cm^2.

53. The method of claim 47, wherein said first direction is opposite said second direction.

54. The method of claim 47, wherein said photodiode is part of a CMOS imager.

55. The method of claim 47, wherein said photodiode is part of a CCD imager.

56. A method of forming a p-n-p photodiode, said method comprising:

forming at least one field oxide region in a substrate;

forming a transistor gate over said substrate and spaced apart from said at least one field oxide region;

forming a first p-type doped layer in said substrate;

forming a photoresist layer over said transistor gate and said field oxide region;

patterning said photoresist layer to form a first opening extending between a first location and a second location, said first location corresponding to a first point over a photodiode area and said second location corresponding to a second point over said field oxide region;

conducting a first angled implant through said first opening to form a p-type surface layer in said first p-type doped layer, said p-type surface layer being laterally displaced from an electrically active area of a gate structure formed over said substrate; and

conducting a second angled implant to form an n-type doped region in said first p-type doped layer, said n-type doped region being located below said p-type surface layer.

57. The method of claim 56, wherein said p-type surface layer is displaced laterally from said electrically active area of said transistor gate by a predetermined distance.

58. The method of claim 56, wherein said predetermined distance is of about 0 Angstroms to about 5,000 Angstroms.

59. The method of claim 56, wherein said p-type surface layer has an implant dose within the range of from about 1 x 10^{12} to about 1 x 10^{14} atoms per cm^2.

60. The method of claim 56, wherein said n-type doped region has an implant dose within the range of from about 1 x 10^{11} to about 1 x 10^{14} atoms per cm^2.

61. The method of claim 56, wherein said p-n-p photodiode is part of a CMOS imager.

62. The method of claim 56, wherein said p-n-p photodiode is part of a CCD imager.